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ZEE, EDWARD	

ART UNIT	PAPER NUMBER
2135	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/791,934	COCCHI ET AL.	
	Examiner	Art Unit	
	Edward Zee	2135	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *03 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/13/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to the original filing of March 3rd, 2004. Claims 1-26 are pending and have been considered below.

Claim Objections

2. Claims 1-18 are objected to because of the following informalities: the Examiner notes that these claims recite several modules "for" performing various functions, which may render the claims unclear and indefinite. It is recommended that the claim language be modified to read "a first module configured to receive..." or the like. Appropriate correction is required.

3. The Examiner further notes that this informality occurs throughout the claims and requests for the Applicant's cooperation in correcting any errors of which applicant may become aware of in the claim language.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 12 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claims 12 and 13 recite the limitation "the interface processor" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 2, 4-13, 15, 16, 19-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Schier (6,907,123).

Claim 1: Schier discloses a conditional access module, for controlling access to a media program via a receiver communicably coupleable to the conditional access module, comprising:

a. a first processor*(ie. multiple processing units to perform decryption)* [column 4, lines 18-24];

b. a second processor*(ie. multiple processing units to perform decryption)* [column 4, lines 18-24];

c. and an interface module*(ie. central processing unit)*, communicatively coupled to the first processor and the second processor, the interface module for processing all communications with the conditional access module*(ie. device)* and externally manifesting a single virtual processor*(ie. encryption decryption engine may comprise a single processor or multiple processors)* to the receiver.

Claim 2: Schier discloses the apparatus of claim 1, and further discloses that the first processor performs a subset of functions to control access to the media program and the second processor

performs a second subset of functions to control access to the media program*(ie. parallel processing of decryption by multiple processors)* [column 4, lines 19-24].

Claim 4: Schier discloses the apparatus of claim 1, and further discloses that the interface module comprises:

a. a first module for receiving conditional access module messages*(ie. communication interface 24)* [figure 2];

b. and a second module for interpreting the received messages and for generating first processor messages for the first processor and second processor messages for the second processor from the received messages*(ie. cpu 20)* [figure 2].

Claim 5: Schier discloses the apparatus of claim 4, and further discloses that the interface module comprises:

a. a third module*(ie. data storage 26)* for receiving a first set of response messages generated by the first processor and a second set of response messages generated by the second processor [figure 2];

b. and a fourth module*(ie. user interface)* for generating conditional access module response messages using at least a portion of the first set of response messages and at least a portion of the second set of response messages*(ie. when received audio is decrypted, it will be outputted to the user)* [figure 2].

Claim 6: Schier discloses the apparatus of claim 1, and further discloses that the interface module receives messages from the receiver, interprets the received messages, and generates first processor messages for the first processor and second processor messages for the second processor*(ie. parallel processing of decryption by multiple processors)* [column 4, lines 19-24].

Claim 7: Schier discloses the apparatus of claim 6, and further discloses that the first processor and second processor operate independently*(ie. parallel processing capability amongst multiple processors)* and the interface module generates first processor messages for the first processor and second processor messages for the second processor by alternately directing received messages to the first processor and the second processor*(ie. multiple processing units may perform decryption of a received message using the same or different algorithms simultaneously)* [column 4, lines 14-29].

Claim 8: Schier discloses the apparatus of claim 6, and further discloses that the first processor messages and the second processor messages define a functional allocation between the first processor and the second processor, and wherein the functional allocation is time-varying*(ie. utilizes a timer to calculate when the switch to the next encryption algorithm should be initiated)* [column 7, lines 42-58].

Claim 9: Schier discloses the apparatus of claim 8, and further discloses that the functional allocation is time varied according to a clock*(ie. timer)* [column 7, lines 42-58].

Claim 10: Schier discloses the apparatus of claim 8, and further discloses that the received messages include encrypted data and the functional allocation is time varied according to the encrypted data*(ie. utilizes a timer to calculate when the switch to the next encryption algorithm should be initiated)* [column 7, lines 42-58].

Claim 11: Schier discloses the apparatus of claim 6, and further discloses that the interface module receives a first set of response messages generated by the first processor and a second set of response messages generated by the second processor and generates conditional access response messages using at least a portion of the first set of response messages and at least a

portion of the second set of response messages*(ie. when received audio is decrypted, it will be outputted to the user)* [figure 2].

Claim 12: Schier discloses the apparatus of claim 1, and further discloses that wherein the interface processor is a processor*(ie. cpu 20)* [figure 2].

Claim 13: Schier discloses the apparatus of claim 1, and further discloses that the interface processor is a hardware state machine*(ie. device implemented using several disparate encryption methods(ie. state) in synchronization with each other)* [column 3, lines 22-26].

Claim 15: Schier discloses the apparatus of claim 1, and further discloses that the first processor and the second processor are communicatively coupled to a shared programming control module*(ie. cpu 20)* [figure 2].

Claim 16: Schier discloses the apparatus of claim 1, and further discloses that the first processor and the second processor each include it's own separate components selected from the group comprising: voltage supply; clock; coprocessor; read only memory; and random access memory*(ie. SRAM, DRAM, etc.)* [column 3, lines 57-67].

Claims 19 and 25: Schier discloses a method and apparatus of controlling access to a media program, comprising the steps of:

a. receiving a message in a conditional access module from a receiver, the message comprising encrypted information to be decrypted by operations independently performed by a both a first processor and a second processor in the conditional access module*(ie. multiple processing units to perform decryption of received message, such as encrypted audio data)* [column 4, lines 18-24];

b. generating first processor commands and second processor commands from the message and providing the first processor commands to the first processor and the second processor commands to the second processor*(ie. parallel processing of decryption commands by multiple processors)* [column 4, lines 19-24];

c. receiving a first processor response from the first processor*(ie. resulting decrypted message after decrypting by multiple processors)* [column 4, lines 19-24];

d. receiving a second processor response from the second processor*(ie. resulting decrypted message after decrypting by multiple processors)* [column 4, lines 19-24];

e. and generating a conditional access message response from at least a portion of the first processor response and the second processor response*(ie. when received audio is decrypted, it will be outputted to the user)* [figure 2].

Claims 20 and 26: Schier discloses the method and apparatus of claims 19 and 25, and further discloses that the encrypted information is a control word packet*(ie. encryption switch signal)* and the conditional access message response is a control word*(ie. device calculates when to switch to the next encryption algorithm utilizing a timer)* [column 7, lines 49-54].

Claim 21: Schier discloses the method of claim 19, and further discloses that the first processor and the second processor operate independently*(ie. parallel processing capability amongst multiple processors)* and wherein the step of generating first processor commands and second processor commands from the message comprises the steps of: alternately directing received messages to the first processor and the second processor*(ie. multiple processing units may perform decryption of a received message using the same or different algorithms simultaneously)* [column 4, lines 14-29].

Claim 22: Schier discloses the method of claim 21, and further discloses that the first processor messages and the second processor messages define a functional allocation between the first processor and the second processor and wherein the functional allocation is time varying*(ie. utilizes a timer to calculate when the switch to the next encryption algorithm should be initiated)* [column 7, lines 42-58].

Claim 23: Schier discloses the method of claim 22, and further discloses that the functional allocation is time varied according to a clock*(ie. timer)* received externally from the conditional access module [column 7, lines 42-58].

Claim 24: Schier discloses the method of claim 22, and further discloses that the received messages include encrypted data and the functional allocation is time varied according to the encrypted data*(ie. utilizes a timer to calculate when the switch to the next encryption algorithm should be initiated)* [column 7, lines 42-58].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schier (6,907,123) in view of Gungl et al. (5,912,453).

Claim 3: Schier discloses the apparatus of claim 1, and further discloses that the multiple processors are communicatively coupled to multiple storage memories*(ie. DRAM, SRAM, etc.)* [column 3, lines 57-67], but does not explicitly disclose that:

a. the first processor is communicatively coupled to a first processor memory;

b. the second processor is communicatively coupled to a second processor memory;

c. and wherein the first processor memory is isolated from the second processor and the second processor memory is isolated from the first processor.

However, Gungl et al. discloses a similar multi-processors decryption apparatus and further discloses that each processor has its own memory which is isolated from the other processors*(ie. processor unit and memory unit are placed on one chip card so that each memory unit isolated from other processors)* [column 3, lines 29-44].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize isolated memory in the apparatus disclosed by Schier in order to ensure the greatest possible security by preventing unauthorized access to the linked memory units as suggested by Gungl et al. [column 3, lines 29-44].

Claims 17 and 18: Schier discloses the apparatus of claim 1, but does not explicitly disclose that the first processor and the second processor include separate logical and physical address ranges.

However, Gungl et al. discloses a similar multi-processors decryption apparatus and further discloses that each processor includes separate logical and physical address ranges*(ie. initial address and end address range)* [column 4, lines 34-59].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize separate memory address ranges in the apparatus disclosed by Schier in order

to ensure the greatest possible security by preventing unauthorized access to the linked memory units as suggested by Gungl et al. [column 4, lines 34-59].

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schier (6,907,123) in view of Thompson (6,163,721).

Claim 14: Schier discloses the apparatus of claim 1, but does not explicitly disclose that the first processor and the second processor are communicatively coupled to a shared charge pump.

However, Thompson discloses a similar multi-processor apparatus and further discloses that the processors are communicatively coupled to a shared charge pump*(ie. charge pump circuit)* [column 4, lines 19-59].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a shared charge pump in the apparatus disclosed by Schier in order or to provide different voltages to the processors and the other modules of the apparatus as suggested by Thompson [column 4, lines 19-59].

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ishihara et al. (2003/0110154) discloses a method of traffic management amongst multiple processors performing encryption and decryption [pages 1-2, paragraph 0011].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Zee whose telephone number is (571) 270-1686. The examiner can normally be reached on Monday through Thursday 9:00AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Y. Vu can be reached on (571) 272-3859. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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